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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,140	02/17/2004	William E. Dougherty JR.	YOR920030437US1 (8728-653	9678

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EXAMINER	
DINH, PAUL	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,140	DOUGHERTY ET AL.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-10,13 and 14* is/are rejected.

7)☒ Claim(s) *3, 11-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This FINAL office action is a response to the amendment + remarks filed on 7/5/06. The remarks are not persuasive; therefore, the rejections based on the prior art of record are maintained.

Claims 1-14 are pending.

Claim Objections

Claims 1 and 13-14 are objected to because (a) it is not clear what is meant by "structural metric" and (b) "structural metric" is not defined in claims 1 and 13-14.

Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form The basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 4-5, 7-9, and 13-14 are rejected under 35 U.S.C. 102(e) as being anticipated by the prior art of record Sanie et al (US Pub. 2004/0210856)

(Claim 1 and similarly recited claims 13-14)

Creating a structural metric prior to physical design (fig 3, element 306, insofar structural metric is understood), the structural metric being proportional to a routability of the circuit design model after the physical design (fig 3, para. 0043); and

Using the structural metric during logic synthesis (fig 3) to create an optimized circuit design model (abstract, para 0042-0044, claim 1).

(Claims 4-5) wherein using the structural metric during logic synthesis comprises using the structural metric during a technology independent synthesis stage of the logic synthesis (fig 1, 3, para 0005, 0009, 0039); during the technology mapping stage of the logic synthesis (fig 1, 3, para 0005-0005-0009).

(Claims 7-8) further comprising incrementally updating the structural metric when logic changes are made to the circuit design model (fig 1-3); wherein incrementally updating the structural metric when logic changes are made to the circuit design model comprises performing recomputation on circuits involved in an optimization and circuits affected by the optimization to provide a structural metric cost (fig 3).

(Claim 9) wherein incrementally updating the structural metric when logic changes are made to the circuit design model comprises maintaining information regarding circuits affected by an optimization, which are computed when recomputation of the structural metric is necessary (fig 1-3).

2. Claims 1-2, 4-7, 9-10, 13-14 are rejected under 35 U.S.C. 102(b) as being Anticipated by the prior art of record Higashida (USP 6006023)

(Claim 1 and similarly recited claims 13-14)

Creating a structural metric prior to physical design (fig 9-19 show structural metric, insofar structural metric is understood), the structural metric being proportional to a routability of the circuit design model after the physical design (fig 9-19, col 2 line 25+, col 4 lines 5-8); and

Using the structural metric during logic synthesis to create an optimized circuit design model (fig 1, 11-12, 17-19).

(Claim 2) wherein using the structural metric during logic synthesis to create an optimized circuit design model comprises adding, deleting or substituting one or more circuits using a combination of Boolean, algebraic and electrical optimizations to create an optimized circuit design model (fig 1-12, 17-19).

(Claims 4-5) wherein using the structural metric during logic synthesis comprises using the structural metric during a technology independent synthesis stage of the logic synthesis (fig 11-12, 19); during the technology mapping stage of the logic synthesis (fig 11-12, 19).

(Claim 6) wherein using the structural metric during logic synthesis comprises using the structural metric during a buffering stage of the logic synthesis (fig 1, 4, 9-13, 15-16, 19)

(Claims 7, 9) further comprising incrementally updating the structural metric when logic changes are made to the circuit design model (fig 1-19); logic changes are made to the circuit design model comprises maintaining information regarding circuits affected by an optimization, which are computed when recomputation of the structural metric is necessary (fig 1, 3, 11-19).

(Claim 10) wherein creating the structural metric comprises creating any one of a distance metric, a sum-of-all-pairs-min-cut ("SAPMC"), and an expansion metric (fig 1-6, 9-12, 17-19).

Response to Applicant Remarks

Turning to Sanie, The applicants state that Sanie does not disclose the claimed "structural metric" and in Sanie fig 3, the "Cell library including Mask Cost Metric" is entirely different from a structural metric being proportional to a routability of a circuit design.

Here are examiner answers:

The claimed "structural metric" is best understood as "Cell library including Mask Cost Metric 306" in fig 3 of Sanie. Note that "structural metric" is not defined in claims 1 and 13-14. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

This "Cell library including Mask Cost Metric 306" (interpreted as the claimed "structural metric") being proportional to a routability of a circuit design (being proportional to a routability of a circuit design is performed by the "Physical Processing 303" also in fig 3 of Sanie where the "Cell library including Mask Cost Metric 306" ("structural metric") being created prior to physical design/processing 303.

Turning to Higashida, the applicants state that Higashida does not disclose or suggest "Using the structural metric **during** logic synthesis to create an optimized circuit design model"

Here are examiners answers:

The limitation "Using the structural metric **during** logic synthesis to create an optimized circuit design model" in claims 1, 13-16; (*and further note that; i.e., claims 4-6 recite "wherein using the structural metric **during** logic synthesis comprises using the structural metric **during** a technology independent synthesis stage/technology mapping stage/ buffer stage of the logic synthesis*) are disclosed in Higashida at the following locations, i.e.,

Col 1 lines 26-35, i.e., "logic synthesis tool applied the buffer tree"

Col 10: "The Seventh Preferred Embodiment

In the first to sixth preferred embodiments, the logic circuit after logic synthesis which has the buffer trees added by the logic synthesis tool is inputted in Step 101 and the optimization of the buffer trees is performed. The method of this optimization may be incorporated in the logic synthesis Tool" (The method of this optimization may be incorporated in the logic synthesis Tool = the claimed "during synthesis *to create an optimized circuit design model*")"; and

"FIG. 12 is a flow chart showing a method of optimizing the logic circuit incorporated in the logic synthesis tool in accordance with the seventh preferred embodiment, where the optimization process (Step 100) for buffer trees of the first to sixth preferred embodiments is incorporated in the flow Of the operation of the logic synthesis .... Incorporating the process (Step 100) into the algorithm of operation of the logic synthesis tool allows sharing ..." (this teaching of Higashida equivalently suggests the claimed limitation "*during synthesis to create an optimized circuit design model*" in claims 1 and 13-14).

The application, the claims, and the remarks have been fully considered, fully reconsidered. The prior art of record discloses all the elements in claims 1-2, 4-10, and 13-14 as detailed and explained above.

Allowable Subject Matter

Claims 3 and 11-12 are objected to as being dependent upon a rejected base claim, but would be allowable if:

a. The above-mentioned claim objection is overcome; and

b. Rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3 and 11-12 would be allowable because the prior art of record does not teach or suggest the limitations in claim 3 and claim 11.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Jack Chiang can be reached on 571-272-7483. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PAUL DINH
PRIMARY EXAMINER

Paul Dinh